REMARKS

By the present amendment and response, claims 1, 4, 6, and 16 have been amended to overcome the Examiner's objections and claim 2 has been canceled. Thus, claims 1, 3-8, and 16-20 remain in the present application. Reconsideration and allowance of pending claims 1, 3-8, and 16-20 in view of the following remarks are requested.

A. Rejection of Claims 1-2, 4-5, 7-8, 16, and 18-20 under 35 USC §102(a)

The Examiner has rejected claims 1-2, 4-5, 7-8, 16, and 18-20 under 35 USC §102(a) as being anticipated by U.S. patent number 6,620,713 to Arghavani et al. ("Arghavani"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 1 and 16, is patentably distinguishable over Arghavani.

The present invention, as defined by amended independent claim 1, includes, among other things, forming a first polysilicon layer over a high-k dielectric, where the first polysilicon layer is formed by utilizing a precursor that does not comprise hydrogen, and forming a second polysilicon layer over the first polysilicon layer. As disclosed in the present application, a gate electrode stack, which includes first and second polysilicon layers, is formed over a high-k dielectric layer. As disclosed in the present application, the first polysilicon layer is formed over the high-k dielectric layer in a deposition process that does not utilize a precursor that comprises hydrogen. By way of example, the first

polysilicon layer can be formed by using an atomic layer deposition process, which can utilize silicon tetrachloride as a precursor.

As disclosed in the present application, the second polysilicon layer in the gate electrode stack can be formed over the first polysilicon layer in a conventional deposition process that uses a precursor, such as silane, that comprises hydrogen. However, since the first polysilicon layer does not comprise hydrogen, the first polysilicon layer acts as a blocking layer to prevent hydrogen in the second polysilicon layer from detrimentally reacting with the high-k dielectric layer. Thus, by utilizing a hydrogen-free polysilicon layer as a blocking layer to prevent hydrogen in a second polysilicon layer from reacting with a high-k dielectric layer, the present invention advantageously prevents FET performance degradation that can occur when a polysilicon gate electrode layer comprising hydrogen is situated on a high-k dielectric layer.

In contrast, Arghavani does not teach, disclose, or suggest forming a first polysilicon layer over a high-k dielectric, where the first polysilicon layer is formed by utilizing a precursor that does not comprise hydrogen, and forming a second polysilicon layer over the first polysilicon layer. Arghavani specifically discloses MOS transistor 200 including high-k dielectric layer 212, silicon interfacial layer 214, and polysilicon gate electrode 216, where high-k dielectric layer 212 is formed on semiconductor substrate 210, silicon interfacial layer 214 is formed on high-k dielectric layer 212, and polysilicon gate electrode 216 is formed on silicon interfacial layer 214. See, for example, column 5, lines 50-57 and Figure 3 of Arghavani. In Arghavani, silicon interfacial layer 214, which

is a silicon layer, is hydrogen-free and has a thickness such that it is sufficient to protect high-k dielectric layer 212 from interacting with the hydrogen components that may exist during the deposition of polysilicon gate electrode 216. See, for example, Arghavani, column 6, lines 30-44.

Thus, in Arghavani, silicon interfacial layer 214 is situated between polysilicon gate electrode 216 and high-k dielectric layer 212. However, silicon interfacial layer 214 comprises silicon, not polysilicon. Also, polysilicon gate electrode 216 comprises only a single layer of polysilicon, which may comprise hydrogen. However, Arghavani fails to teach, disclose, or even suggest a gate electrode stack comprising first and second polysilicon layers, where the first polysilicon layer is formed by utilizing a precursor that does not comprise hydrogen and is situated over a high-k dielectric layer.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by amended independent claim 1, is not taught, disclosed, or suggested by Arghavani. Thus, amended independent claim 1 is patentably distinguishable over Arghavani. As such, the claims 3-8 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Arghavani for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The present invention, as defined by amended independent claim 16, includes, among other things, forming a gate electrode layer over a high-k dielectric layer, where the gate electrode layer comprises a first layer of polysilicon situated over a second layer

of polysilicon, and where the first layer of polysilicon in the gate electrode layer is formed by utilizing a precursor that does not comprise hydrogen. Amended independent claim 16 recites similar limitations as amended independent claim 1 discussed above. Thus, for similar reasons as discussed above, amended independent claim 16 is also patentably distinguishable over Arghavani. Thus claims 17-20 depending from amended independent claim 16 are, *a fortiori*, also patentably distinguishable over Arghavani for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Rejection of Claims 1, 3, 16, and 17 under 35 USC §102(b)

The Examiner has rejected claims 1, 3, 16, and 17 under 35 USC §102(b) as being anticipated by U.S. patent number 6,451,641 to Halliyal et al. ("Halliyal"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 1 and 16, is patentably distinguishable over Halliyal.

In contrast to the present invention as defined by amended independent claims 1 and 9, Halliyal does not teach, disclose, or suggest forming a first polysilicon layer over a high-k dielectric, where the first polysilicon layer is formed by utilizing a precursor that does not comprise hydrogen, and forming a second polysilicon layer over the first polysilicon layer. Halliyal specifically discloses MOSFET 100 including high-k gate dielectric material layer 108 situated on p-doped silicon substrate 102 and gate electrode

110 situated on high-k gate dielectric material layer 108. See, for example, column 5, lines 47-51 and Figure 1 of Halliyal. In Halliyal, gate electrode 110 comprises polysilicon or polysilicon-germanium and is formed under non-reducing conditions, which include providing a hydrogen-free source of silicon to a CVD apparatus. See, for example, Halliyal, column 7, lines 8-15.

Thus, in Halliyal, gate electrode 110 comprises polysilicon or polysilicon-germanium, which can be formed using a hydrogen-free source of silicon. However, Halliyal fails to teach, disclose, or remotely suggest a first polysilicon layer over a high-k dielectric, where the first polysilicon layer is formed by utilizing a precursor that does not comprise hydrogen, and forming a second polysilicon layer over the first polysilicon layer, as specified in amended independent claim 1. In fact, Halliyal fails to teach, disclose, or suggest a gate electrode stack comprising first and second layers of polysilicon.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by amended independent claim 1, is not taught, disclosed, or suggested by Halliyal. Thus, amended independent claim 1 is patentably distinguishable over Halliyal. As such, the claim 3 depending from amended independent claim 1 is, *a fortiori*, also patentably distinguishable over Halliyal for at least the reasons presented above and also for additional limitations contained in the dependent claim.

The present invention, as defined by amended independent claim 16, includes, among other things, forming a gate electrode layer over a high-k dielectric layer, where

the gate electrode layer comprises a first layer of polysilicon situated over a second layer of polysilicon, and where the first layer of polysilicon in the gate electrode layer is formed by utilizing a precursor that does not comprise hydrogen. Amended independent claim 16 recites similar limitations as amended independent claim 1 discussed above. Thus, for similar reasons as discussed above, amended independent claim 16 is also patentably distinguishable over Halliyal. Thus claim 17 depending from amended independent claim 16 is, *a fortiori*, also patentably distinguishable over Halliyal for at least the reasons presented above and also for additional limitations contained in the dependent claim.

C. Rejection of Claim 6 under 35 USC §103(a)

The Examiner has rejected claim 6 under 35 USC §103(a) as being unpatentable over Arghavani. However, as discussed above, amended independent claim 1 is patentably distinguishable over Arghavani. Thus, claim 6 depending from amended independent claim 1 is, *a fortiori*, also patentably distinguishable over Arghavani for at least the reasons presented above and also for additional limitations contained in the dependent claim.

D. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1 and 16 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 3-8, and 16-20

pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1, 3-8, and 16-20 pending in the present application is respectfully requested.

Attorney Docket No.: 0180146

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 12/23/04

Michael Farjami, Esq.
Reg. No. 38,135

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

CERTIFICATE OF FACSIMILE TRANSMISSION
I hereby certify that this correspondence is being filed by facsimile transmission to United States Patent and Trademark Office at facsimile number **703-872-9306** on the date stated below. The facsimile transmission report indicated that the facsimile transmission was successful.

Date of Facsimile: 12-23-2004

LESLEY L. LAM
Name of Person Performing Facsimile Transmission

12-23-04
Signature Date

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date of Deposit:

Name of Person Mailing Paper and/or Fee

Signature Date